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L1	1576	(storage or disk or memory) with (copy\$4 or mirror\$4) with pair	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:39
L2	0	I1 and (((graphic\$2 or user)near interface) or diplay\$4 or view\$4) with (storage or memory or disk) with (resource\$4 or source) with target with pair\$4)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:00
L3	3	(((graphic\$2 or user)near interface) or diplay\$4 or view\$4) with (storage or memory or disk) with (resource\$4 or source) with target with pair\$4)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:01
L4	282	(storage or disk or memory) with (copy\$4 or mirror\$4) with pair and (user with interface)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:39
L5	122	(storage or disk or memory) with (copy\$4 or mirror\$4) with pair and (user with interface) and (error with (messag\$4 or alert\$4))	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:40
L6	6	I5 and (pair\$4 with (rule\$2 or condition\$4 or criteria\$4))	US-PGPUB; USPAT; JPO; IBM_TDB	OR	OFF	2006/04/27 23:42

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disk **column** 磁盘卷标. Disk working **storage** 磁盘工作储存空间. diskette 软磁碟 ... event

object 事件对象. event **Pair High Event Pair High** ...

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1 Flow analysis for verifying properties of concurrent software systems

Matthew B. Dwyer, Lori A. Clarke, Jamieson M. Cobleigh, Gleb Naumovich
October 2004 **ACM Transactions on Software Engineering and Methodology (TOSEM)**,
Volume 13 Issue 4

Publisher: ACM Press

Full text available: [pdf\(1.13 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This article describes FLAVERS, a finite-state verification approach that analyzes whether concurrent systems satisfy user-defined, behavioral properties. FLAVERS automatically creates a compact, event-based model of the system that supports efficient dataflow analysis. FLAVERS achieves this efficiency at the cost of precision. Analysts, however, can improve the precision of analysis results by selectively and judiciously incorporating additional semantic information into an analysis. We report o ...

Keywords: Dataflow analysis, finite-state verification, model checking

2 Large-scale circuit placement

Jason Cong, Joseph R. Shinnerl, Min Xie, Tim Kong, Xin Yuan
April 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 10 Issue 2

Publisher: ACM Press

Full text available: [pdf\(428.15 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Placement is one of the most important steps in the RTL-to-GDSII synthesis process, as it directly defines the interconnects, which have become the bottleneck in circuit and system performance in deep submicron technologies. The placement problem has been studied extensively in the past 30 years. However, recent studies show that existing placement solutions are surprisingly far from optimal. The first part of this tutorial summarizes results from recent optimality and scalability studies of exi ...

Keywords: Placement, large-scale optimization, optimality, scalability

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